



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/056,287	01/23/2002	Burnell G. West	M-12401 US	9790
7590 12/10/2003			EXAMINER	
Deborah Winocur 4057 Amaranta Avenue Palo Alto, CA 94306			LE, JOHN H	
			ART UNIT	PAPER NUMBER
			2863	

DATE MAILED: 12/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/056,287

Applicant(s)

WEST, BURNELL G.

Examiner

John H Le

Art Unit

2863

WU

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

1) ☐ Responsive to communication(s) filed on \_\_\_\_\_.

2a) ☒ This action is FINAL.

2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

4) ☒ Claim(s) 1-32 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.

6) ☒ Claim(s) 1-32 is/are rejected.

7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.

8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on 16 April 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. §§ 119 and 120

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some \* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

## Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.

4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: \_\_\_\_\_.

***Respons to Amendment***

1. This office action is in response to applicant's amendment received on 10/27/2003.

Claims 1, 6, 7, 8, 10, 20, and 26 have been amended.

Claims 33-42 have been cancelled.

***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1, 10, 20, and 26 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 1, line 7, "a resolution of less than one clock cycle" was not described in the specification.

Claim 10, line 2, "a resolution of less than one clock cycle" was not described in the specification.

Claim 20, line 2, line 9, "a resolution of less than one clock cycle" was not described in the specification.

Claim 26, line 2, "a resolution of less than one clock cycle" was not described in the specification.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (USP 5,642,478) in view of Daum et al. (USP 5,815,634).

Regarding claims 1 and 10, Chen et al. teach a circuit for time stamping events, the circuit comprising: node controller 38, which read on an event stream distributor coupled to receive the primary event stream (38 receiving 44, Fig.1); and a plurality of timestamp circuits (Col.8, lines 6-13, Col.11, lines 43-45, lines 53-55), each timestamp circuit coupled to receive a respective secondary event stream from the event stream distributor (38 distributing second event, Fig.1).

Chen et al. fail to teach time stamping an event with a resolution of less than one clock cycle.

Daum et al. teach time stamping an event with a resolution of less than one clock cycle (e.g. Col.8, lines 4-17).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include step of time stamping an event with a resolution of less than one clock cycle as taught by Daum et al. in a distributed trace data acquisition system of Chen et al. for the purpose of providing a step controller for an audio/video

Art Unit: 2863

playback system which maintains audio and video data streams in substantial synchronization during step control (Daum et al., Col.4, lines 30-33).

6. Claims 1-5 and 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adelman et al. (USP 4,894,823) in view of Daum et al. (USP 5,815,634).

Regarding claims 1 and 10, Adelman et al. teach a circuit for time stamping events, the circuit comprising: a digital line interface unit 117, which read on an event stream distributor coupled to receive signal from a receive access module 116, which read on the primary event stream (117 receiving 116, Fig.1); and a plurality of timestamp circuits (Col.2, lines 5-26, Col.6, lines 3-8), each timestamp circuit coupled to receive a respective secondary event stream 118 from the event stream distributor 117 (117 distributing second event 118, Fig.1).

Regarding claims 2 and 11, Adelman et al. teach an event rate in each of the secondary event streams is lower than an event rate in the primary event stream (Col.5, lines 62-67).

Regarding claims 3 and 12, Adelman et al. teach the relative timing of the events in the primary event stream is maintained in each of the secondary event streams (Col.2, lines 5-26, Col.6, lines 3-8).

Regarding claims 4 and 13, Adelman et al. teach the primary event stream is a differential signal (116-1 through 116-X, Col.5, lines 51-61).

Regarding claims 5 and 14, Adelman et al. teach the secondary event streams are differential signals (118-1 through 118-x, Col.5, lines 62-67).

Art Unit: 2863

Adelmann et al. fail to teach time stamping an event with a resolution of less than one clock cycle.

Daum et al. teach time stamping an event with a resolution of less than one clock cycle (e.g. Col.8, lines 4-17).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include step of time stamping an event with a resolution of less than one clock cycle as taught by Daum et al. in a time stamping for packet system of Adelmann et al. for the purpose of providing a step controller for an audio/video playback system which maintains audio and video data streams in substantial synchronization during step control (Daum et al., Col.4, lines 30-33).

7. Claims 26-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fransson (USP 5,940,467) in view of Daum et al. (USP 5,815,634).

Regarding claims 26-29, Fransson teaches a counting circuit, the circuit comprising: a first counter 31 coupled to receive the signal (Fig.1); and a first plurality of gates 71, 72, 73, 74, 75, 76, each gate of the first plurality of gates coupled to receive the signal and each gate of the first plurality of gates coupled to receive a respective control signal from the first counter 31 (Fig.2, Fig.5A), wherein the first plurality of gates are AND gates, wherein the signal is a differential signal, wherein the signal is a single-ended signal (Col.4, lines 39-65, Col.7, lines 32-67).

Regarding claim 30, Fransson teaches the counter is a Johnson counter (Col.2, lines 5-7).

Regarding claim 31, Fransson teaches the counter is an N-bit counter (Col.2, lines 5-7, Col.4, lines 14-19, Col.5, lines 43-45).

Regarding claim 32, Fransson teaches a second counter 50-1, 50-2, 50-3, 50-4 coupled to receive the primary event stream (Fig.2); and a second plurality of gates of registers 99-1, 99-2, 99-3, 99-4, each gate of the second plurality of gates coupled to receive the signal and each gate of the second plurality of gates coupled to receive a respective control signal from the second counter (Fig.8, Col.12, lines 45-65).

Fransson fails to teach time stamping an event with a resolution of less than one clock cycle.

Daum et al. teach time stamping an event with a resolution of less than one clock cycle (e.g. Col.8, lines 4-17).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include step of time stamping an event with a resolution of less than one clock cycle as taught by Daum et al. in a counting circuit of Fransson for the purpose of providing a step controller for an audio/video playback system which maintains audio and video data streams in substantial synchronization during step control (Daum et al., Col.4, lines 30-33).

8. Claims 20-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boerker (US 2003/0035502 A1) in view of Daum et al. (USP 5,815,634).

Regarding claim 20, Boerker teaches a data reception circuit for receiving a serial input data stream with a high data transfer rate, the method comprising: receiving the primary event stream 1; a data stream separation circuit 4 distributing rising edge



Art Unit: 2863

events in the primary event stream among a first plurality of secondary event streams ([0057]); a asynchronously clocked register array 8 recording an arrival time of each event in the first plurality of secondary event streams with respect to a reference clock ([0058]); the data stream separation circuit 4 distributing falling edge events in the primary event stream among a second plurality of secondary event streams ([0057]); and recording an arrival time of each event in the second plurality of secondary event streams with respect to the reference clock ([0058]).

Regarding claim 21, Boerker teaches an event rate in each secondary event stream of the first plurality and the second plurality of secondary event streams is lower than an event rate in the primary event stream ([0057]).

Regarding claim 22, Boerker teaches the primary event stream is a differential signal ([0055]).

Regarding claim 23, Boerker teaches each secondary event stream of the first plurality and the second plurality of secondary event streams are differential signals ([0055]).

Regarding claim 24, Boerker teaches distributing rising edge events comprises selectively enabling a first plurality of gates and distributing falling edge events comprises selectively enabling a second plurality of gates ([0066]).

Regarding claim 25, Boerker teaches distributing rising edge events comprises selectively enabling a first plurality of gates using a first counter 8 that is clocked by the primary event stream and distributing falling edge events comprises selectively enabling



Art Unit: 2863

a second plurality of gates using a second counter 17 that is clocked by the primary event stream ([0067]).

Boerker fails to teach time stamping an event with a resolution of less than one clock cycle.

Daum et al. teach time stamping an event with a resolution of less than one clock cycle (e.g. Col.8, lines 4-17).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include step of time stamping an event with a resolution of less than one clock cycle as taught by Daum et al. in a data reception circuit of Boerker for the purpose of providing a step controller for an audio/video playback system which maintains audio and video data streams in substantial synchronization during step control (Daum et al., Col.4, lines 30-33).

9. Claims 6-9, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adelman et al. (USP 4,894,823) in view of Daum et al. (USP 5,815,634) as applied to claims 1 and 10 above, and further in view of Boerker (US 2003/0035502 A1).

Regarding claims 6 and 7, Adelman et al. and Daum et al. (USP 5,815,634) fail to teach distributing events in the primary event stream comprises selectively enabling a plurality of gates using a counter that is clocked by the primary event stream such that a first event in the primary event stream passes through a first gate, a second event in the primary event stream passes through a second gate, and so on until an Nth event in the primary event stream passes through an Nth gate, wherein N is a positive integer.

Boerker teaches distributing events in the primary event stream comprises selectively enabling a plurality of gates using a counter that is clocked by the primary event stream such that a first event in the primary event stream passes through a first gate, a second event in the primary event stream passes through a second gate, and so on until an Nth event in the primary event stream passes through an Nth gate, wherein N is a positive integer ([0056], [0060], [0066], Fig.1, Fig.2).

Regarding claim 8, Boerker teaches distributing rising edge events in the primary event stream among a first plurality of secondary event streams; and distributing falling edge events in the primary event stream among a second plurality of secondary event streams ([0057]).

Regarding claims 9 and 19, Boerker teaches registering the events in each of the secondary event streams ([0055]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include step of distributing events in the primary event stream comprises selectively enabling a plurality of gates using a counter that is clocked by the primary event stream as taught by Boerker in a time stamping for packet system nodes of Adelman et al. in view of Daum et al. for the purpose of providing an increasing transfer rate, data or information is transferred via a transfer channel in shorter and shorter times (Boerker, [0005]).

10. Claims 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adelman et al. (USP 4,894,823) in view of in view of Daum et al. (USP 5,815,634) as applied to claim 10 above, and further in view of Fransson (USP 5,940,467).

Regarding claims 15-18, Adelman et al. and Daum et al. fail to teach a first counter coupled to receive the primary event stream; and a first plurality of gates coupled to the first counter, wherein the first counter is a Johnson counter, wherein the first counter is an N-bit counter, a second counter coupled to receive the primary event stream; and a second plurality of gates coupled to the second counter, a plurality of registers, each register operable to register events of one or more secondary event streams.

Fransson teaches a first counter 31 coupled to receive the primary event stream; and a first plurality of gates 71, 72, 73, 74, 75, 76 coupled to the first counter (Fig.1, Fig.2, Fig.3A), wherein the first counter is a Johnson counter, wherein the first counter is an N-bit counter (Col.2, lines 5-7), second counters 50-1, 50-2, 50-3, 50-4 coupled to receive the primary event stream (Fig.2); and a second plurality of gates of registers 99-1, 99-2, 99-3, 99-4 coupled to the second counter, each register operable to register events of one or more secondary event streams (Fig.8, Col.12, lines 45-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a counter, plurality of gates coupled to the counter, wherein the counter is a Johnson counter, wherein the counter is an N-bit counter as taught by Fransson in a time stamping for packet system nodes of Adelman et al. in view of Daum et al. for the purpose of providing a counting circuit, the resolution of which is equal to the cycle time of the first clock signal applied to the counting circuit (Fransson, Col.2, lines 46-48).

### ***Response to Arguments***

Art Unit: 2863

11. Applicant's arguments filed 09/22/2003 have been fully considered but they are not persuasive.

-Applicant argues that the prior did not teach "time stamping an event with a resolution of less than one clock cycle".

-“Time stamping an event with a resolution of less than one clock cycle” was not described in the specification. Claims 1, 10, 20, and 26 have been rejected under 35 U.S.C. 112, first paragraph as discussed above.

- Daum et al. teach time stamping an event with a resolution of less than one clock cycle (e.g. Col.8, lines 4-17).

### ***Conclusion***

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Art Unit: 2863

13. Specifically Daum et al. has been added to second ground of rejection.

***Contact Information***

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John H. Le whose telephone number is (703) 605-4361.

The examiner can normally be reached on 9:00 - 5:30.

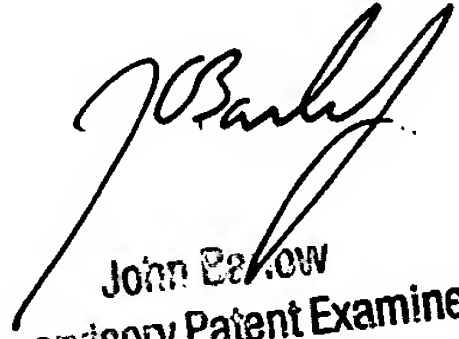
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E. Barlow can be reached on (703) 308-3126. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

John H. Le

Patent Examiner-Group 2863

December 1, 2003

  
John E. Barlow  
Supervisory Patent Examiner  
Technology Center 2800